AND8023/D

Implementing the NCP1200 in Low-Cost AC/DC Converters

Prepared by: **Christophe Basso**
ON Semiconductor

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch–off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part–count is the key parameter, particularly in low–cost AC/DC adapters, auxiliary supplies etc. Thanks to its proprietary Very High–Voltage Integrated Circuit (VHVIC) technology, ON Semiconductor NCP1200 will please experts as well as non–experts in the Switch–Mode Power Supplies (SMPS) arena as the following features demonstrate:

- **No need of auxiliary winding:** the VHVIC technology lets you supply the IC directly from the high–voltage DC rail. We call it Dynamic Self–Supply (DSS). In battery charger applications, you no longer need to design a special primary circuitry to cope with the transient lack of auxiliary voltage (e.g. when Vout is low).
- **Short–circuit protection:** by permanently monitoring the feedback line activity, the IC is able to detect the presence of a short–circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation. For given applications (e.g. constant output power supplies), you can easily disconnect this protective feature.
- **Low standby–power:** if SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un–needed switching cycles, the NCP1200 drastically reduces the power wasted during light load conditions. In no–load conditions, the NPC1200 allows the total standby power to easily reach next International Energy Agency (IEA) recommendations.
- **No acoustic noise while operating:** instead of skipping cycles at high peak currents, the NCP1200 waits until the peak current demand falls below a user–adjustable 1/3rd of the maximum limit. As a result, cycle skipping can take place without having a singing transformer … You can thus select cheap magnetic components free of noise problems.
- **External MOSFET connection:** by leaving the external MOSFET external to the IC, you can select avalanche proof devices which, in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).
- **SPICE model:** a dedicated model to run transient cycle–by–cycle simulations is available but also an averaged version to help you closing the loop. Ready–to–use templates can be downloaded in OrCAD's PSpice, INTUSOFT's IsSpice and Spectrum–Software's μCap from the ON Semiconductor web site, www.onsemi.com, NCP1200 related section.
- **Low external part–count:** by integrating the principal electronic blocks in one die, the final NCP1200 implementation reveals an obvious gain in component reduction compared to other offers:
  - Built–in clock generator without external R–C elements. Operating frequencies at 40 kHz, 60 kHz or 100 kHz.
  - The optocoupler is directly wired to the feedback pin, the internal IC control taking care of the signal flow.
  - The 250 ns Leading Edge Blanking (LEB) circuitry also saves an external R–C network.

Dynamic Self–Supply

To avoid the use of a dissipative resistor, NCP1200 implements a controlled current source whose technology allows a direct connection to the high–voltage rail (up to 450 VDC). Figure 1a depicts the component arrangement. The current source always operates in the ON or OFF states, either delivering 4 mA or zero. As a result, the internal V_{CC} pin ramps up and down with a 2 V ripple centered around 10.6 V (Figure 1b).

April, 2001 – Rev. 3

Publication Order Number:
AND8023/D

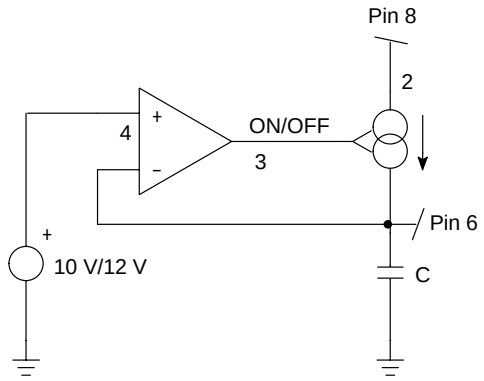

Figure 1a. Internal Implementation of the Dynamic Self–Supply

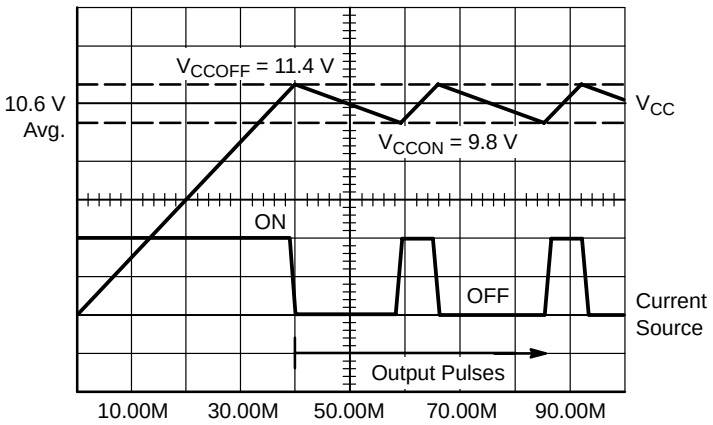

Figure 1b. DSS Waveforms During Start–Up and Normal Mode (CV_{CC} = 10 μF)

As one can see from Figure 1a, the current source supplies the IC and the Vcc capacitor. Thanks to the circuitry nature, the current source duty–cycle will automatically adjust depending on the IC average current consumption. Because this is a controlled source, this current stays constant whatever the high–voltage rail excursion (V_{HV}): from 100 VDC up to 370 VDC. The IC contribution to the total SMPS power budget is therefore: $V_{HV} \cdot I_{pin8}$.

The internal IC consumption is made of the internal electronic blocks (clock, comparators, driver etc.) but also depends on the MOSFET's gate charge, Qg. If we select a MOSFET like the MTD1N60E, Qg equals 11 nC (max) and with a maximum switching frequency of 48 kHz, the average current necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:

$$Fsw \cdot Qg = 530\ \mu A$$

Fsw = maximum switching frequency (Hertz)
Qg = MOSFET's gate charge (Coulomb)

If we now add this number to the normal IC consumption, we reach a typical total of 1.2 mA. The total IC power contribution alone is therefore: 330 V . 1.2 mA = 396 mW.

Decreasing the Standby Power

Below stands the future stand–by power recommendations issued by International Energy Agency (IEA). It concerns stand–by power when there is no output power demand:

Rated Input Power	Phase 1, January 2001	Phase 2, January 2003	Phase 3, January 2005
> 0.3 W and < 15 W	1.0 W	0.75 W	0.30 W
≥ 15 W and < 50 W	1.0 W	0.75 W	0.50 W
≥ 50 W and < 75 W	1.0 W	0.75 W	0.75 W

A typical 4 W universal mains AC/DC wall adapter using the NCP1200 will exhibit a no–load power consumption of less than 380 mW @ Vin = 230 VAC. If a lower power consumption is required, you have several options to achieve it:

1. Use a MOSFET with lower gate charge Qg, but as we saw the driver's contribution is small.
2. Connect pin 8 through a diode to one of the mains input to apply a rectified half–wave on pin 8. Since we have either 4.0 mA or 0 synchronized with this half–sine wave, we should integrate the V–I product over a cycle to obtain the final average power. However, depending on the V_{CC} capacitor, we may have some half–sine portions where the current source if OFF: the V_{CC} capacitor level has not reached $UVLO_{Low}$ and the current source is left opened. To simplify the curves, we can assume a constant current flowing through pin 8 (actually the total NCP1200 consumption + a few losses) and integrate over a half–sine only. This leads to the final formula: $Pavg = \frac{2 * Vmainspeak * Iavg\ (Pin\ 8)}{\pi}$. Our previous number drops to 250 mW. If you carefully look at Figure 2a, you will notice that the reverse voltage is sustained by the diode bridge. The maximum anode voltage of the Dstart diode is also clamped at the high–voltage rail. Therefore, a standard fast diode like the 1N4148 can safely be used in this option. However, because of the lack of synchronization between the DSS and the mains, it is necessary to equilibrate the diode voltage when both diode and DSS are inactive. This can be done by wiring a 220 kΩ in parallel with the diode. Otherwise, a standard 1N4937 can also do the job without any resistor in parallel…

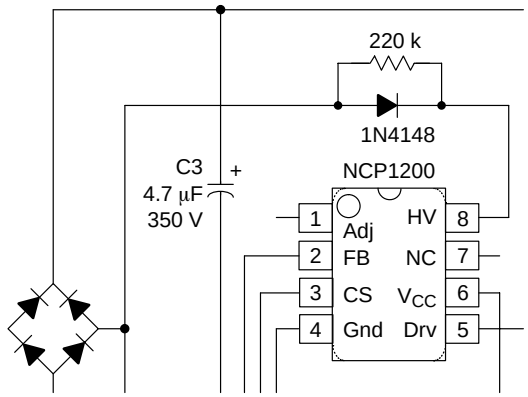

Figure 2a. A simple diode naturally reduces the average voltage on pin 8.

Figure 2b depicts the V_{CC} voltage obtained when using this method. Despite the lack of synchronization between the mains and the DSS, the average V_{CC} level is not affected.

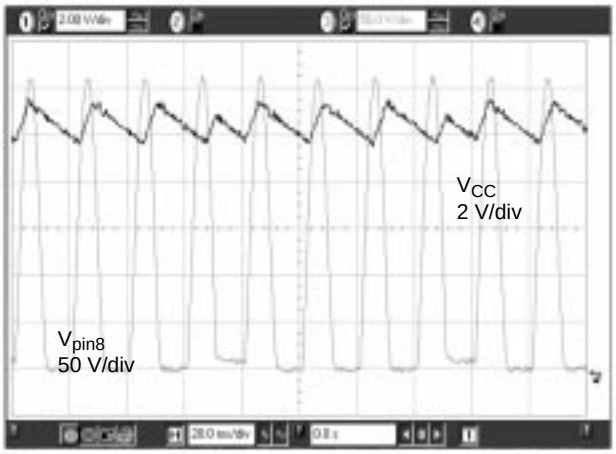

Figure 2b. By wiring a diode in series with pin 8, you do not affect the average V_{CC} level.

3. If you permanently force the V_{CC} level above V_{CCOFF} with an auxiliary winding, you will automatically disconnect the internal start–up source and the IC will be fully self–supplied from this winding. Again, the total power drawn from the mains will significantly decrease. However, make sure the auxiliary voltage never exceeds the 16 V limit, particularly in overshoot transients (e.g. the load is suddenly removed). To avoid this trouble and also implement an efficient Over Voltage Protection (OVP), Figure 3 schematic offers a possible solution:

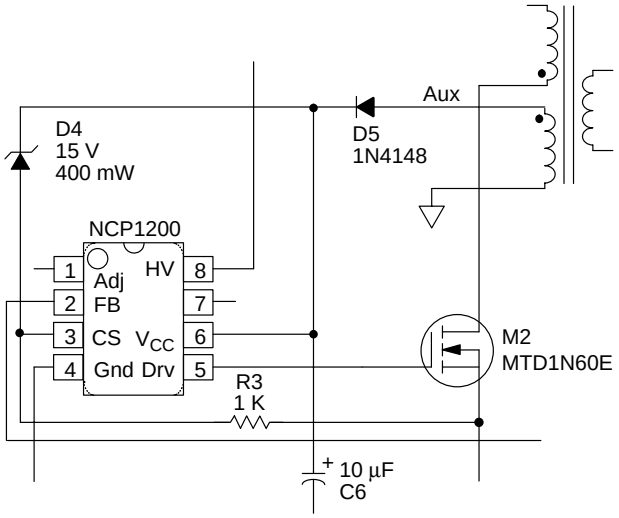

Figure 3. By wiring an auxiliary winding, you further decrease the standby power.

The typical operating voltage can be set at 12 V, with an overvoltage protection at 15 V. As a benefit, if the optocoupler fails, the SMPS turns into primary regulation mode and prevents any output voltage runaway. Typical measurements using this method gave a standby power of 84 mW at 230 VAC.

Skip Cycle Mode

The NCP1200 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin (pin 2). In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so–called skip cycle mode, also named controlled burst operation. Because this operation takes place at low peak currents, you will not hear any acoustic noise in your transformer. Figure 4a depicts how the IC implements the cycle skipping while Figure 4b shows typical switching patterns at different load levels.

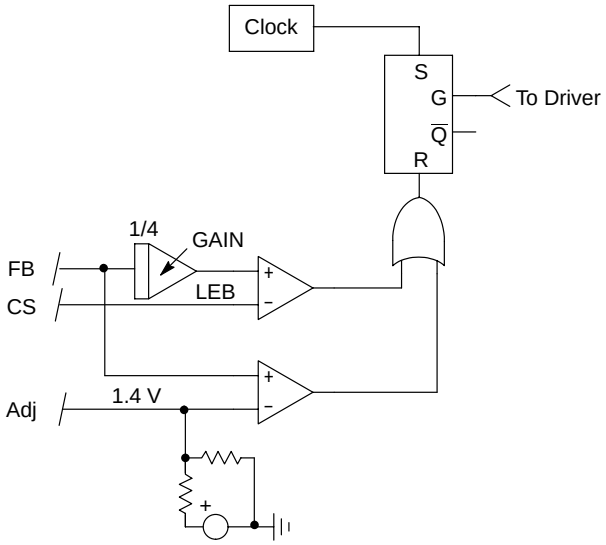

Figure 4a. NCP1200 Skip Cycle Implementation

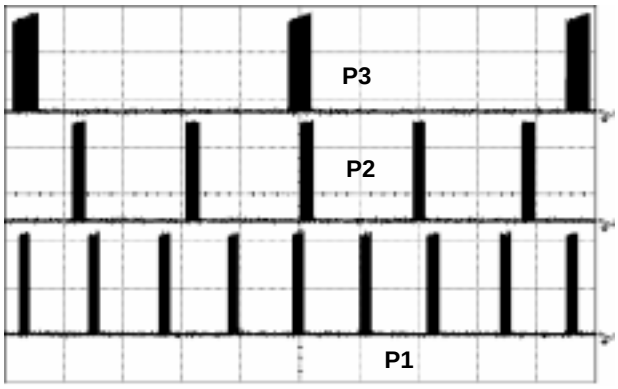

Figure 4b. Output pulses at various power levels (X = 5 μs/div) P3 < P2 < P1

When FB is above the skip cycle threshold (1.4 V by default), the peak current cannot exceed 1 V/Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1/4, 350 mV/Rsense by default (Figure 4c). The user still has the flexibility to alter this 1.4 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level.

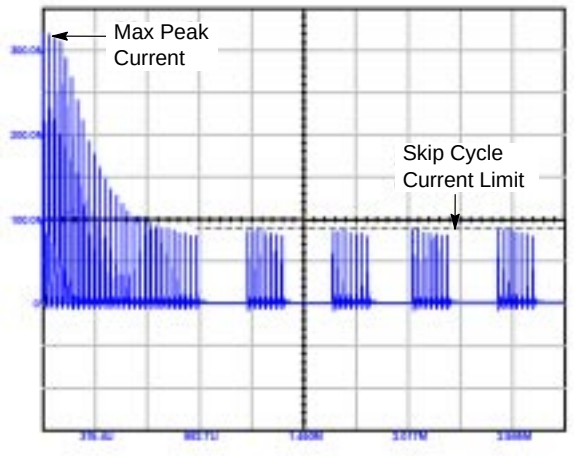

Figure 4c. The skip cycle takes place at low peak currents which guarantees noise–free operation.

The power transfer now depends upon the width of the pulse bunches (Figure 4b). Suppose we have the following component values:

Lp, primary inductance = 1 mH
Fsw , switching frequency = 48 kHz
Ip skip = 300 mA (or 350 mV/Rsense)

The theoretical (η = 100%) power transfer is therefore:

$$\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw = 2.16\ W \qquad \text{(eq. 2)}$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 2.1 . 0.1 = 216 mW.

Skip Adjustment

By altering the DC voltage present on pin 1, you have the ability to adjust the current level at which skip cycle operation will take place. By default, skip cycle occurs when the peak current demand falls below one third of the maximum peak current. If your design needs to enter standby at a higher or lower current (e.g. for noise reasons), you can alter the internal setpoint by imposing a different level than 1.4 V on pin 1. This can be achieved by using a resistor bridge between V_{CC} and ground. Pin 1 impedance is typically 25 kΩ.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is mandatory to implement a true short–circuit protection. A short–circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.8V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, the NCP1200 hosts a dedicated overload detection scheme. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty–cycle. The system recovers when the fault condition disappears.

During the start–up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time–out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the V_{CCOFF} (typically 11.4 V) the device internally watches for an overload current situation. If this condition is still present when the V_{CCON} is reached, the controller stops the driving pulses, prevents the self–supply current source to restart and puts all the circuitry in standby, consuming as little as 350 μA typical (I_{CC3} parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 6.3 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 11.4 V and again delivers output pulses at the V_{CCOFF} crossing point. If the fault condition has been removed before V_{CCON} approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 5 shows the evolution of the signals in presence of a fault.

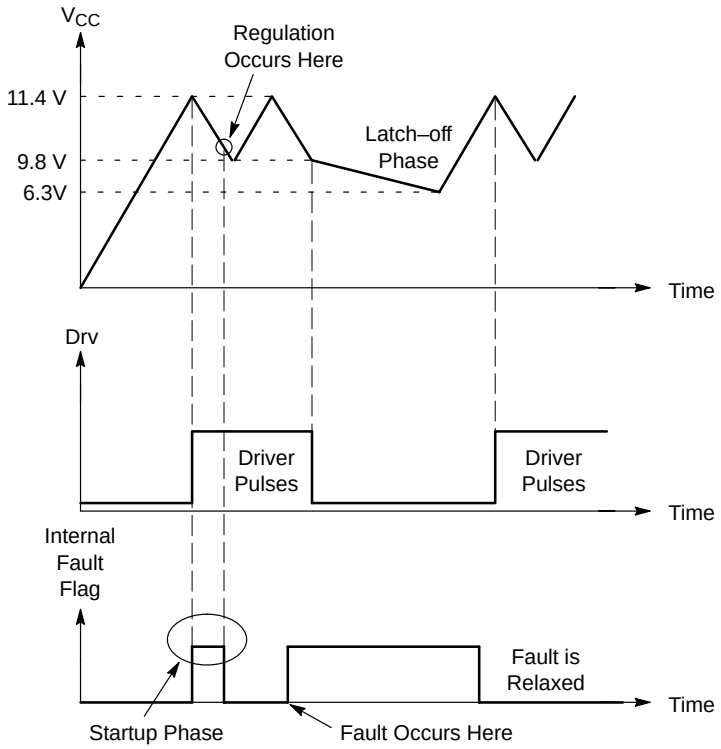

Figure 5. If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes. If the fault still persists when V_{CC} reached $UVLO_L$, then the controller enters burst mode until recovery.

* Always make sure that the output power you are looking for asks for an FB level less than the maximum value to avoid a false overload circuitry trigger.
* Because of component dispersions (NCP1200 frequency span, Rsense tolerance etc.), the overload protection will not be active as soon as you exceed the nominal power by a small amount. If you shoot for a given Pout, it is likely that the overload protection activates at roughly twice this value, especially if you implement a low–gain single zener feedback loop. You need to be sure that the output components sustain the corresponding current. Fortunately, because of temperature, the transformer core permeability will decrease as well as the primary inductance. This means less maximum power at higher temperatures.

Deactivating the Overload Detection

By wiring a 20 kΩ resistor from FB to ground, you permanently deactivate the overload protection circuitry. This is a very useful feature, especially if you need to build a constant output power converter.

Power Dissipation

The NCP1200 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1200 current consumption. The total power dissipation can be evaluated using: $(V_{HVDC} - 11\ V) \times I_{CC2}$. If we operate the device on a 250 VAC rail, the maximum rectified voltage can go up to 350 VDC. As a result, the worse case dissipation occurs on the 100 kHz version which will dissipate 340 . 1.8 mA @ Tj = 25°C = 612 mW (however this 1.8 mA number will drop at higher operating temperatures). A DIP8 package offers a junction–to–ambient thermal resistance $R_{\theta J-A}$ of 100°C/W. The maximum power dissipation can thus be computed knowing the maximum operating ambient temperature (e.g. 70°C) together with the maximum allowable junction temperature (125°C): $P_{max} = \frac{Tj_{max} - TA_{max}}{R_{\theta J-A}} = 550\ mW$. As we can see, we do not reach the worse consumption budget imposed by the 100 kHz version. Two solutions exist to cure this trouble. The first one consists in adding some copper area around the NCP1200 DIP8 footprint. By adding a min–pad area of 80mm^2 of 35µ copper (1 oz.), $R_{\theta J-A}$ drops to about 75°C/W which allows the use of the 100 kHz version. The other solutions are a) add a series diode with pin 8 (as suggested in the above lines) to drop the maximum input voltage down to 225 V (707/π) and thus dissipates less than 410 mW b) implement a self–supply through an auxiliary winding to permanently disconnect the self–supply.

SO–8 package offers a worse $R_{\theta J-A}$ compared to that of the DIP8 package: 178°C/W. Again, adding some copper area around the PCB footprint will help decreasing this number: 12mm x 12mm to drop $R_{\theta J-A}$ down to 100°C/W with 35µ copper thickness (1 oz.) or 6.5mm x 6.5mm with 70µ copper thickness (2 oz.). As one can see, we do not recommend using the SO–8 package for the 100 kHz version with DSS active as the IC may not be able to sustain the power (except if you have the adequate place on your PCB). However, using the solution of the series diode or the self–supply through the auxiliary winding does not cause any problem with this frequency version.

Calculating the V_{CC} Capacitor for Overload

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 11.4 V to 9.8 V? The required time depends on the start–up sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 11.4 V to 10 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.5 mA, we can calculate the required capacitor using the following formula: $\Delta t = \frac{\Delta V \cdot C}{i}$, with ΔV = 2 V (eq. 3). Then for a wanted Δt of 10 ms, C equals 8 µF or 10 µF for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 350 µA typical. This happens at V_{CC} = 10 V and it remains stuck until V_{CC} reaches 6.3 V: we are in latch–off phase. Again, using the calculated 9.8 µF and 350 µA current consumption, this latch–off phase lasts: 109 ms.

Protecting the Power MOSFET

If the leakage inductance is kept low, an avalanche rugged MOSFET such as the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high–voltage spike superimposed over the mains, without the help of a clamping network. However, if this leakage path permanently forces a drain–source voltage above the MOSFET BVdss (e.g. 600 V), a clamping network is mandatory and must be built around a passive RC network or a Transient Voltage Suppressor (TVS). Figure 6a depicts the phenomenon while the below lines details the calculation steps:

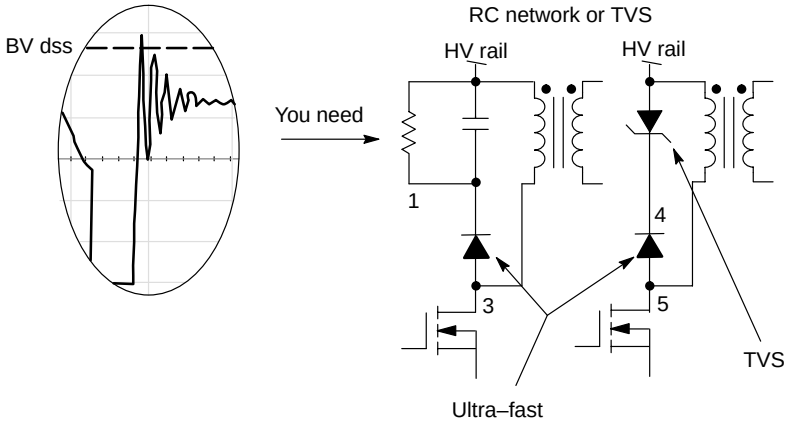

Figure 6a. Care must be taken to ensure a safe operation of the MOSFET

1. RC Network

The RC network will permanently impose a fixed clamping level that will oppose to the leakage voltage. As a result, the drain will be clamp to V_{HVrail} + Vclamp. You normally select a clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

To calculate the component values, the following formula will help you:

$$Rclamp = \frac{2 \cdot Vclamp \cdot (Vclamp - (Vout + Vf\,sec) \cdot N)}{Lleak \cdot Ip^2 \cdot F_{SW}} \quad \text{(eq. 4)}$$

$$Cclamp = \frac{Vclamp}{Vripple \cdot F_{SW} \cdot Rclamp} \quad \text{(eq. 5)}$$

The power dissipated by Rclamp can also be expressed by:

$$P_{Rclamp} = \frac{1}{2} \cdot Lleak \cdot Ip^2 \cdot F_{SW} \cdot \frac{\frac{Vclamp}{(Vout + Vf\,sec) \cdot N}}{\frac{Vclamp}{(Vout + Vf\,sec) \cdot N} - 1}$$

with:

Vclamp: the desired clamping level.

Ip: the maximum peak current (e.g. during overload)

Vout + Vf: the regulated output voltage level + the secondary diode voltage drop

Lleak: the primary leakage inductance

N: the Ns:Np conversion ratio

Fsw: the switching frequency

Vripple: the clamping ripple, could be around 20 V

2. Transient Voltage Suppressor

Despite the low–cost offered by the above RC solution, the clamping level unfortunately varies with the peak current. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. If the peak power is really high, then turn to a 1.5 KE200 which accepts up to 1.5 kW @ 1 ms.

Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

3. Snubber Network

Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn–off. The peak voltage at which the leakage forces the drain is calculated by: $V_{max} = Ip \cdot \sqrt{\frac{Lleak}{Clump}}$ (eq. 6) where Clump represents the total parasitic capacitance seen at the MOSFET opening. Depending on the output power, you can either wire a simple capacitor across the MOSFET or an R–C network, as shown by Figure 6b.

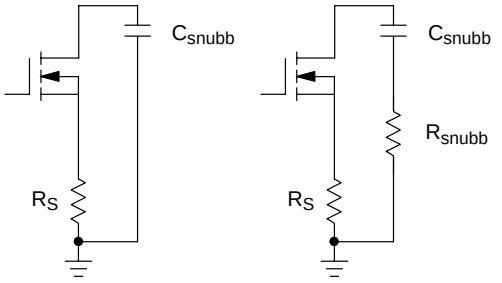

Figure 6b. If the output power is low, you can wire a simple capacitor MOSFET's drain and ground.

To calculate the values of this RC snubber, you need to measure the ringing frequency imposed by the leakage inductance and all the stray capacitances. Make sure you use a low capacitance probe, otherwise you might affect the observed frequency. Once you have it, calculate the impedance of the leakage inductance at the ringing frequency: $Z = 2 \cdot \pi \cdot F_{ring} \cdot L_{leak}$ (eq. 7). Wiring a resistor R whose value equals Z should solve the problem but at the expense of a large power dissipation. To lower the dissipated heat, you can wire a capacitor C in series with R: $C = \frac{1}{\pi \cdot F_{ring} \cdot R}$ (eq. 8). If the output power is low, you can directly wire this capacitor between the MOSFET drain and ground (not between drain–source to avoid substrate injection). Unfortunately, you discharge this capacitor in the MOSFET every time it turns on... Further tweaking is thus necessary to tune the dissipated power versus standby power.

ON Semiconductor Protection Devices

SMPS protection clearly needs fast switching components to ensure a reliable operation in the event of dangerous transients. ON Semiconductor portfolio offers a comprehensive list of semiconductors dedicated to protection: fast diodes, zeners, TVS etc. Below is a small list of typical component you can select to protect the MOSFET in your application. The complete list of TVS devices can be found at the following URL: *www.onsemi.com* or by ordering the selection guide TVSPROMO1299/D by sending an email to: ONlit@hibbertco.com:

Clipping Elements

Reference	Nominal Voltage (V)	Average Power (W)	Maximum Peak Power
1N5953B	150	1.5	98 W @ 1 ms
1N5955B	180	1.5	98 W @ 1 ms
1N5383B	150	5.0	180 W @ 8.3 ms
1N5386B	180	5.0	180 W @ 8.3 ms
1N5388B	200	5.0	180 W @ 8.3 ms
P6KE150A	150	5.0	600 W @ 1 ms
P6KE180A	180	5.0	600 W @ 1 ms
P6KE200A	200	5.0	600 W @ 1 ms
1.5KE150A	150	5.0	1.5 kW @ 1 ms
1.5KE180A	180	5.0	1.5 kW @ 1 ms
1.5KE200A	200	5.0	1.5 kW @ 1 ms

Fast Diodes

Reference	V_{RRM}	Ton (typical)	IF max
MUR160	600 V	50 ns	3 A
MUR1100E	1000 V	25 ns	3 A
1N4937	600 V	200 ns	1 A
MSR860*	600 V	100 ns	8 A
MSRB860–1*	600 V	100 ns	8 A

*Soft recovery diodes

Calculating the Component Values for a Typical Application

Suppose that we would like to build a simple AC/DC wall adapter with an NCP1200 delivering a raw DC voltage with the following specs:

- Pout = 3.5 W
- Target efficiency: η = 75% $\rightarrow$ Pin = 4.66 W
- Vout = 6 V, Rload = 10.3 Ω, Iout = 580 mA
- V_{AC}in = 100 VAC to 250 VAC

The first step lies in calculating the peak rectified value obtained from this line range:

$$\rightarrow Vin_{peak} = Vin \cdot \sqrt{2} - 2 \cdot Vf \text{ with :} \qquad \text{(eq. 9)}$$

Vin: the AC input voltage
Vf: a forward drop of a bridge diode, 0.7 V @ Id

$\rightarrow Vin_{peak}$ = 140 V at low line
$\rightarrow Vin_{peak}$ = 352 V at high line

Bulk Capacitor

The bulk capacitor supplies the high–frequency current pulses to the SMPS, while it is refueled at low rate by the mains. Figure 7a shows a typical rectifying configuration. However, the bulk capacitor should be dimensioned to provide enough energy between the line peaks. The worse case appears at the lowest line level combined with the maximum output current. Figure 7b depicts the voltage waveform observed over C_{bulk} in Figure 7a example.

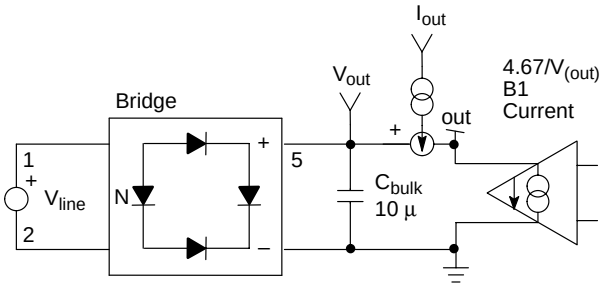

Figure 7a. A Full–Wave Rectification Configuration

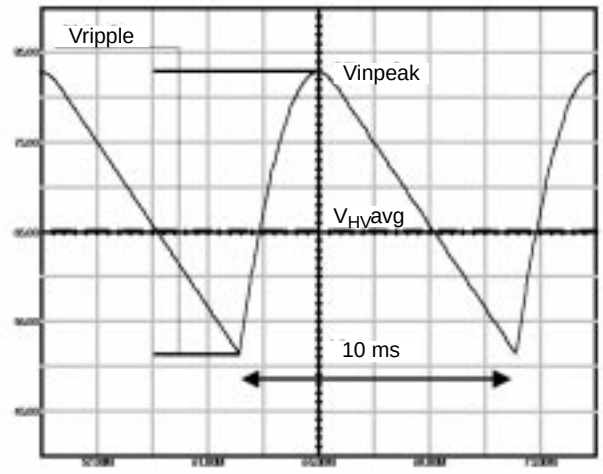

Figure 7b. A Typical Ripple Voltage over the Bulk Capacitor

To simplify the calculation, we will neglect the charging period and thus consider a total discharge time equal to $\frac{1}{2 \cdot Fline}$. From the design characteristics, we can evaluate the equivalent current (Iload) drawn by the charge at the lowest input line condition. Let's us adopt a 40% ripple level, or a 50 V drop from the corresponding Vin_{peak}. To evaluate the equivalent load current (which discharges Cbulk between the peaks), we divide the input power by the average rectified voltage: $Iload = \frac{Pin}{Vrect_{avg}} = \frac{Pout}{\eta \cdot \left(Vpeak - \frac{Vripple}{2}\right)}$ (eq. 10) = 46 mA @ 100 VAC input voltage. Thanks to Figure 7b information, we can evaluate the capacitor value which allows the drop from Vpeak down to Vavg – (Vripple/2) to stay within our 50 V target: $dV \cdot C = i_{load} \cdot dt$:

$$Cbulk = \frac{Pout}{2 \cdot \eta \cdot Fline \cdot Vripple \cdot \left(Vpeak - \frac{Vripple}{2}\right)}$$

= (eq. 11) 9.3 µF or 10 µF for a normalized value.

High–voltage DC Rail Range

From the above formula, we can extract the ripple amplitude at any line level:

$$Vripple = Vpeak \cdot \left(1 - \sqrt{1 - \frac{Pout}{Cbulk \cdot \eta \cdot Fline \cdot Vpeak^2}}\right) \qquad \text{(eq. 12)}$$

Let us now calculate the final average DC value delivered to the SMPS at high but also low line:

$$V_{HVavg} = Vin \cdot \sqrt{2} - 2 \cdot Vf - \frac{Vripple}{2} \qquad \text{(eq. 13)}$$

$\rightarrow$ 115 VDC @ 100 VAC with a 50 Vpp ripple (initial target)
$\rightarrow$ 343 VDC @ 250 VAC with 19 Vpp ripple (calculated)

To confirm the validity of our calculation, a simple SPICE simulation can be run where the load is replaced by a current source. However, thanks to the feedback loop of the converter, the input current will vary depending on the line level. To avoid tweaking the current source at different line levels, Figure 7a's B1 element computes the input current according to the required power: $Iload = \frac{P_{SMPS}}{Vbulk}$ exactly as the final SMPS would do. Simulations gave a 29 Vpp ripple at low line (VHVavg = 126 V), turning into 12 Vpp at high line (VHV_{avg} = 342 V). The calculations gave less pessimistic results simply because we have neglected the capacitor re–charge time which reduces its discharge time.

Diode Bridge Selection

To select the right rectifiers, it is necessary to know the RMS current flowing through its internal diodes. Prior to reach this final result, we need to evaluate the diode conduction time. From Figure 8a, we can see that the diode starts to conduct when V_{AC}in reaches Vmin and stops when reaching Vin_{peak}:

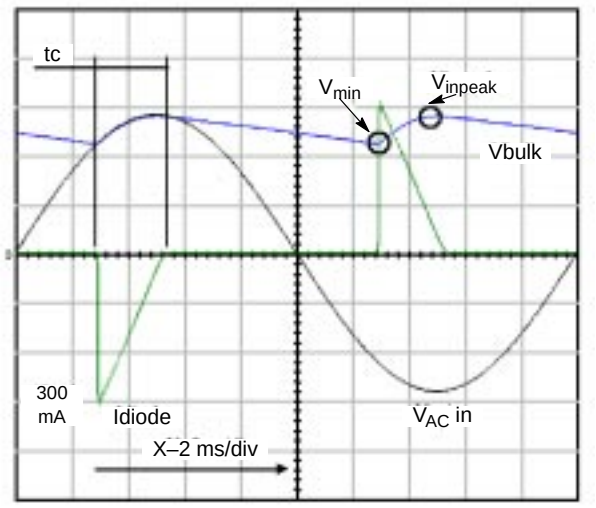

Figure 8a. When V_{AC}in reaches Vpeak, the diode stops conducting.

From a mathematical point of view, we can calculate the time V_{AC}in takes to reach Vmin:

$V_{AC}in \cdot \sin(\omega \cdot t) = Vmin$. Since Vpeak is reached at the input sinusoid top (or one fourth of the input period), then the diode conducting time tc is simply: $tc = \frac{1}{4 \cdot Fline} - \frac{\sin^{-1}\left(\frac{V\,min}{V_{AC}in \cdot \sqrt{2}}\right)}{360 \cdot Fline}$ = 2.1 ms @ Vin = 100 VAC (eq. 14). During these 2.1 ms, Vbulk is the seat of a rising voltage equal to Vripple or 29 Vpp. This corresponds to a brought charge Q of: $Qbulk = Vripple \cdot Cbulk = 290\ \mu C$ (eq. 15).

From Figure 8a, we can calculate the amount of charge Q drawn from the input by integrating the input current over the diode conduction time: $Qin = \int_0^{tc} i_{diode}(t).dt$ (eq. 16). The expression of $i_{diode}(t)$ is: $Ipeak \cdot \frac{tc - t}{tc}$ (eq. 17). After proper integration, it comes: $Qin = \frac{1}{2} \cdot Ipeak \cdot tc$. If we now equate Qbulk and Qin and solve for Ipeak, it comes: $Ipeak = \frac{Qbulk \cdot 2}{tc}$ (eq. 17) or 280 mA peak, as confirmed by the simulation. We can now evaluate the RMS current flowing through the diodes: $Irms = \sqrt{Fline \cdot \int_0^{tc} (idiode(t))^2 \cdot dt} = Ipeak \cdot \sqrt{\frac{tc}{3} \cdot 2 \cdot Fline}$ = (eq. 18) 86 mA @ VAC = 100. A 400 V/1A diode bridge or four 1N4007 can thus be selected for the rectifying function. A small resistor is however put in series to ensure a surge current (when you plug the SMPS in the AC outlet) less than the diode maximum peak current (Ifsm).

Thanks to these numbers, we compute the apparent power at low line: 86 mA x 100 V = 8.6 VA which compared to our 4.66 Watts of active power (neglecting the input diode bridge and Cbulk losses) gives a power factor of: $PF = \frac{W}{V.A} = 0.54$ (eq. 19) conform to what we could expect from this kind of offline power supply. With a reverse voltage of 400 V, you can select either a 1 A/400 V bridge or 4 x 1N4007 diodes.

Transformer Calculation

Transformer calculation can be done in several manners: a) you evaluate ALL the transformer parameters, electrical but also physical ones, including wire type, bobbin stack–up etc. b) you only evaluate the electrical data and leave the rest of the process to a transformer manufacturer. We will adhere to the latest option by providing you with a list of potential transformer manufacturers you can use for prototyping and manufacturing. However, as you will discover, designing a transformer for SMPS is an iterative process: once you freeze some numbers, it is likely that they finally appear either over or under estimated. As a result, you re–start with new values and see if they finally fit your needs. To help you speed–up the transformer design, an Excel® design–aid sheet is available from the ON Semiconductor web site, *www.onsemi.com/NCP1200*. Let's start the process with the turn ratio calculation:

Turn Ratio and Output Diode Selection

The primary/secondary turn ratio affects several parameters:

- The drain plateau voltage during the OFF time: the lowest plateau gives room for the leakage inductance spike before reaching the MOSFET's BVdss: $Vplateau = \frac{Np}{Ns} \cdot (Vout + Vf) + VinDC_{max}$ (eq. 20).
- The secondary diode Peak Inverse Voltage (PIV) is linked to the turn ratio and the regulated output voltage by: $PIV = \frac{Ns}{Np} \cdot VinDC_{max} + Vout$ (eq. 21). If you lower the plateau voltage, you will increase the reverse voltage the secondary diode must sustain.
- The amp–turns equation Np . αIp = Ns . Is should satisfy the average output current demand with $Iout_{avg} = \frac{Ip \cdot toff \cdot Fsw \cdot \alpha}{2 \cdot \frac{Np}{Ns}}$ (eq. 22). The α parameter illustrates the energy diverted by the leakage inductance at the switch opening (take 0.95 for low leakage designs).

With these numbers in mind, you can tweak the turn ratio according to the MOSFET BVdss and the diode. Below are given ON Semiconductor references for Schottky diodes:

Reference	V_{RRM} (V)	Io (A)	Case
MBRM120LT3	20	1.0	PowerMite
MBRM130LT3	30	1.0	PowerMite
MBRA130LT3	30	1.0	SMA
MBRA140LT3	40	1.0	SMA
MBRS120LT3	20	1.0	SMB
MBRS130LT3	30	1.0	SMB
MBRS140LT3	40	1.0	SMB
MBRS190T3	90	1.0	SMB
MBRS1100T3	100	1.0	SMB
MBRS320T3	20	3.0	SMC
MBRS330T3	30	3.0	SMC
MBRS340T3	40	3.0	SMC
MBRS360T3	60	3.0	SMC
1N5817	20	1.0	Axial
1N5818	30	1.0	Axial
1N5819	40	1.0	Axial

*Please see brochure BR1487/D for thermal and package details.

If we select an MBRA140LT3 (V_{RRM} = 40 V), then the PIV should be selected around 35 V at high line: $N = \frac{PIV - Vout}{VinDC_{max}}$ (eq. 23). If we select Np:Ns = 1: 0.08, then PIV = 34 V at 350 VDC input voltage which is okay with the selected diode. The plateau voltage at the drain will establish around 430 VDC: it leaves up to 170 V for the leakage spike.

The average diode Id_{avg} current is the converter's DC output current which is 580 mA, in line with our 1 A MBRA140LT3. The repetitive peak current seen by the diode is: $Ipeak_{sec} = \alpha \cdot Ip \cdot \frac{Np}{Ns}$ (eq. 24). The diode RMS current Id_{rms} can be evaluated using: $Id_{rms} = Ipeak_{sec} \cdot \sqrt{\frac{Fsw \cdot toff}{3}}$ (eq. 25). Finally, the total conduction losses of the diode can be assessed through the following equation: $Pdiode_{avg} = Vf \cdot Id_{avg} + Rd \cdot Id_{rms}^2$ (eq. 26) with Vf the forward drop at Id = $Ipeak_{sec}$ and Rd, the dynamic resistance $\frac{dVf}{dId}$ @Id = $Ipeak_{sec}$.

Once Ip have been evaluated, you will need to confirm the agreement with the diode maximum rating specs.

Primary Inductance and Peak Current

When the SMPS operates in the Discontinuous Conduction Mode (DCM), the sum of the ON and OFF times equal the switching period: $ton + toff = \frac{1}{Fsw}$ (eq. 27). From the FLYBACK equations, we can easily calculate t_{on} and t_{off}. During the ON time, the converter applies VinDC to the primary inductance which forces the current to build up with a slope of $\frac{VinDC}{Lp}$. Because the NCP1200 operates in current–mode, the ON time expires when the current setpoint Ip has been reached: $ton = \frac{Lp \cdot Ip}{VinDC}$ (eq. 28). In DCM, we must satisfy equation 27. That is to say, the OFF time lasts until the core is fully reset or the secondary current has come back to zero: $toff = \frac{Lp \cdot Ip}{N \cdot (Vout + Vf)}$ (eq. 29), with N the turn ratio between the secondary and the primary and Vf the secondary rectifier forward drop at a given current (≈1 V). In a FLYBACK SMPS, the input power flow is evaluated using the formula: $Pin = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw$ (eq. 30) with Lp the primary inductance, Ip the primary current at the end of the ON time and Fsw the converter's switching frequency. Pin is linked to Pout by the efficiency using: $Pin = \frac{Pout}{\eta}$ (eq. 31). Combining equations 27, 28, 29, 30, 31 and solving for Lp we obtain the critical inductance value above which we would go into Continuous Conduction Mode (CCM) at the lowest input voltage $\left(VinDC_{avg} - \frac{Vripple}{2}\right)$ and maximum output power:

$$Lp \leq \left(\frac{N \cdot (Vout + Vf) \cdot VinDC}{N \cdot (Vout + Vf) + VinDC}\right)^2 \cdot \frac{\eta}{2 \cdot Pout \cdot Fsw}$$

(eq. 32). Finally, the peak current corresponding to this inductance value can be computed from equations 30, 31: $Ip = \sqrt{\frac{2 \cdot Pout}{\eta \cdot Lp \cdot Fsw}}$ (eq. 33). With our example data in

mind, the calculation gives a primary inductance of 6.4 mH at Fsw = 40 kHz (nominal NCP1200 switching frequency). The corresponding Ip is 190 mA.

In equation 30, two unknowns exist: Lp and Ip. The above calculations show how to select Lp from a conduction mode point of view (always stay in DCM), which leads to a final operating peak current. However, from equation 6, we can see that a high peak current leads to a large inductance spike when the switch opens. We should then try to work at a low primary peak current to avoid this potentially lethal voltage kick. However, working at a low peak current means a higher primary inductance to satisfy equation 30 which, in turn, induces a larger leakage energy (the leakage inductance is proportional to the square of the primary turns)…We thus need a balance between the low primary current requirements combined with our low leakage inductance needs. Let's go over the whole process and see how we can tweak the parameters, keeping in mind that the lowest turn number also ensures the lowest manufacturing cost…

Step 1:

Evaluate the critical inductance value with eq. 32. Ip is calculated via eq. 33 → Lp = 6.4 mH, Ip = 190 mA.

Step 2:

The NCP1200 limits the peak current to: $\frac{0.9\ V}{Rsense}$ (eq. 34), 0.9 V varying ±10%. We should then select a sense resistor from the E24 series, also affected by a ±5% tolerance, which authorizes the peak current to grow up to the number calculated by eq. 33. The E24 shunt series looks like the following for medium output powers: …0.56 Ω, 0.68 Ω, 0.82 Ω, 1 Ω, 1.2 Ω, 1.5 Ω, 1.8 Ω, 2.2 Ω, 2.7 Ω, 3.3 Ω, 3.9 Ω, 4.7 Ω… As you can see, it will be easier to pick up an available reference from the E24 series then refine the inductance value to reach our goal. This option avoids to freeze the inductance without having the necessary flexibility on the shunt. From step 1 and equation 34, Rshunt = 4.24 Ω. If we select 4.7 Ω, we will have difficulties to reach our peak current with the previous inductance (remember that we cannot increase it otherwise we go into CCM). Another problem would be the FB permanently pushed to the maximum current demand and triggering the overload mode. Therefore, let's select 3.9 Ω from the E24 series and later on diminish the inductance value to fit eq. 30. Now, we need to apply worse cases of tolerance variations to see how they affect the final output power result. To refine the calculation, we will include the NCP1200 overcurrent propagation delay which is 120 ns typical. Propagation delay corresponds to the actual time taken by the internal chain to really pull the MOSFET's gate to ground when the peak current setpoint has been reached. During this time, the primary current keeps growing up with a slope of $\frac{VinDC}{Lp}$ (eq. 36). Figure 9a details this principle.

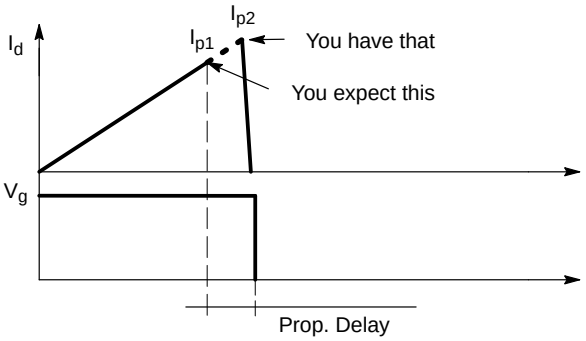

Figure 9a. The NCP1200 propagation delay leads to a slightly higher peak current than expected.

The data we have are: Lp = 6.4 mH ±10%, Fsw = 40 kHz ±15%, Rsense = 3.9 Ω ±5% and $Vsense_{max}$ = 0.9 ±5%. From these values, we can combine worse case together to see a) are we always able to deliver our 3.5 W? b) what is the maximum output power capability?:

$$Pout_{min} = \frac{1}{2} \cdot Lp_{min} \cdot \left(\frac{Vsense_{min}}{Rsense_{max}} + \frac{VinDC_{min}}{Lp_{min}} \cdot t_{prop} \right)^2 \cdot Fsw_{min} \rightarrow 3.3\ W \quad \text{(eq. 37)}$$

$$Pout_{max} = \frac{1}{2} \cdot Lp_{max} \cdot \left(\frac{Vsense_{max}}{Rsense_{min}} + \frac{VinDC_{max}}{Lp_{max}} \cdot t_{prop} \right)^2 \cdot Fsw_{max} \rightarrow 6.3\ W \quad \text{(eq. 38)}$$

From the above numbers, we can see that we cannot deliver the target power in the worse case. Let's reduce the Rsense value to the next reference, 3.3 Ω: (you can use the spreadsheet to speed–up this process)

$Pout_{min}$ = 4.6 W
$Pout_{max}$ = 8.8 W
Rsense = 3.3 Ω, Lp = 6.4 mH

From these results, we can consider that 4.6 W is more than we need. By reducing the inductance value to 5.5 mH, the numbers are updated to:

$Pout_{min}$ = 4 W
$Pout_{max}$ = 7.6 W
Rsense = 3.3 Ω, Lp = 5.5 mH

With this case, the 4 W output power offers a guardband above 14% (4 W compared to 3.5 W) and it will thus leave some dynamic on the FB level without triggering the overvoltage protection circuitry.

Step 3:

This final step should give us the type of transformer we can use for our application. In FLYBACK converters, we need a gap to expand the storage capability of a given un–gapped core. The gap presence imposes a decrease in the remnant flux density Br and allows a larger field excursion before reaching the saturation (a gap does not change the saturation level Bsat nor the coercitive field values Hc). However, the gap is usually made by grinding

the center leg of the selected core (E or RM etc.). This operation can be difficult, especially on small cores used for powers as the one we are looking for. For this reason, most of the manufacturers do not recommend gaps above 0.6 mm. Large gaps also generate fringing flux which can lead to disturbing ElectroMagnetic Interference (EMI) leaks.

Two methods can be used for the design of the transformer depending on the information given by the core manufacturer:

First Method

1. From eq. 34 and Lp value, evaluate the maximum required storage energy capability $Lp_{max}.Ip^2_{max}$.
2. Depending on your application constraints (dimensions, weight etc.) select a given core geometry (E, RM etc.).
3. From the core manufacturer handbook, look at the graph which gives $L.I^2$ versus A_L curves. Draw a horizontal line which corresponds to the above required $L.I^2$ number for the selected geometry. Any core references appearing below this curve can be used. However, in an attempt to minimize the leakage inductance (less primary turns), try to select the largest A_L .
4. Plot a vertical line which passes through the intersection point step 3 created. This gives you the A_L.
5. From the A_L versus air–gap length curve, extract the corresponding air–gap and check if it is machinable (< 600 μm?).
6. From the A_L, calculate the primary turn number with:

$$N = \sqrt{\frac{Lp}{AL}} \qquad \text{(eq. 39)}$$

7. Finally, check that $Bs \cdot N \cdot Ae > Lp_{max} \cdot Ip_{max}$ with Bs the core saturation limit at 100°C and Ae the effective core area. If it fails, reduce the A_L value by keeping the air–gap within reasonable limits and check that the updated turn numbers are still in agreement with the bobbin capability (the transformer manufacturer will normally tell you about it).
8. With the help of the spreadsheet, you have the choice to tweak Lp in order to decrease the turn number to finally reduce the leakage inductance.

Second Method

1. Depending on your application constraints (dimensions, weight etc.) select a given core geometry (E, RM etc.)
2. From the calculated Lp value, evaluate the *minimum* turn number with: $N = \frac{Lp_{max} \cdot Ip_{max}}{Bs \cdot Ae}$ (eq. 40)
3. You now need to calculate the specific inductance value by applying: $AL = \frac{Lp}{N^2}$
4. Evaluate the desired gap length lg (in mm) through the following formula: $lg = \frac{\mu o \cdot \mu a \cdot N^2 \cdot Ae - Lp \cdot lm}{Lp \cdot \mu a} \cdot 1000$ (eq. 41) with μo the air permeability ($4.\pi.10^{-7}$), μa the amplitude permeability (the core permeability at high flux excursions), N the turn number, lm the mean magnetic path length (m).

Numerical Application

For our 3.5 W charger operating a 40 kHz, we have selected an E16 core in B2 material (Thomson–LCC) offering the following parameters:

Ae = 0.0000198m²
Bsat = 300mT @ 100°C
μa > 1000 (T° > 100°C, B = 330mT)
lm = 0.0348 meter

To lower the turn numbers (for leakage but also for winding time reasons), we have purposely decreased the previously calculated Lp value down to 2.7 mH which gives an operating peak current of 290 mA and a sense resistor of 2.7 Ω.

Applying method 1 leads to:

AL = 60 nH/turn²
Np = 212 turns
Ns = 17 turns

The manufacturer will need the primary and secondary RMS currents calculated at the lowest line level:

$$Isec_{rms} = Ipeak_{sec} \cdot \sqrt{\frac{Fsw \cdot toff}{3}} \text{ or } 2.7 \text{ A (eq. 42)}$$

The primary current is obtained with:

$$Iprim_{rms} = Ipeak_{prim} \cdot \sqrt{\frac{Fsw \cdot ton}{3}} \text{ or } 184 \text{ mA (eq. 43)}$$

MOSFET Selection

The transformer being designed, we can look at the MOSFET type. From equation 20, the plateau voltage (during the toff duration) rises up to 438 V. By selecting a 600 V device, we ensure enough headroom for the leakage spike. If this spike is finally too energetic, we can either clamp it with an adequate network or choose a 800 V MOSFET. From equation 43, a 1 A MOSFET is suitable and can be selected from the below devices:

Reference	BVdss (V)	$RDS_{(ON)}$ (Ω)	Peak Current (A)	Package
NTB10N60	600	0.75	–	TO–220
NTB10N60	600	0.75	–	D_2PAK
NTD4N60	600	2.3	–	DPAK
NTP6N60	600	1.1	–	TO–220
NTP6N60	600	1.1	–	D_2PAK
MTP4N80E	800	3.0	4.0	TO–220
MTD1N80E	800	12	1.0	DPAK
MTD1N60E	600	8.0	1.0	DPAK
MTB3N60E	600	2.2	3.0	D_2PAK
MTP2N60E	600	3.8	2.0	TO–220
MTP3N60E	600	2.2	3.0	TO–220
MTP6N60E	600	1.2	6.0	TO–220

Let's pick–up an MTD1N60E which features the following specs:

BVdss = 600 V
$RDS_{(ON)}$ = 13 Ω @ Tj = 100°C
Case = DPAK
$R_{\theta JA}$ = 71 °C/W on min pad area
Max junction temperature = 150°C
Qg = 11 nC max. (V_{GS} = 10 V)
Coss = 40 pF

If we operate at an ambient of 70°C, the maximum power the component can dissipate on free–air is given by: $Pmax = \frac{Tj_{max} - T_A}{R_{\theta JA}}$ = 1.1 W (eq. 45). The total MOSFET losses are a combination of the conduction losses and the switching losses. From equation 43, we can compute the MOSFET conduction losses: $Pcond = RDS_{(ON)} \cdot Id^2_{RMS}$ = 440 mW (eq. 46).

Switching losses appear because of the overlap between drain current and drain–source voltage during transitions. We have losses during the switch closing (P_{sw}on) but also during the switch opening (P_{sw}off). In DCM, the turn–on losses are mainly created by the recurrent discharge of the stray parasitic capacitors in the MOSFET. The MOSFET contributes to these losses via its Coss capacitor. Unfortunately, Coss does not linearly vary with Vds during the transition and an accurate calculation would require the use of an equivalent capacitor, resulting from the Coss integral over the switching period. To simplify the evaluation, we will stick to the classical Coss given in the data–sheet, 40 pF max and neglect the other stray capacitance (e.g. from the transformer or a snubber): $P_{sw}on = \frac{Coss \cdot (Vds_{plateau})^2 \cdot Fsw_{max}}{2}$ (eq. 47) with $Vds_{plateau}$ given by eq. 20. We obtain 175 mW. To estimate this ON transition duration, we can calculate the time t_s needed to push enough Coulomb in the gate to properly bias the MOSFET. However, the time during which the drain falls corresponds to the charging time of the Miller capacitance or the V_{GS} "plateau" duration. This plateau, which occurs at 6 V for the MTD1N60E is not the V_{GS}th parameter (≈3 V). From the MOSFET's gate–charge chart, we can extract the amount of necessary Coulomb Qg2 to cross–over the plateau area: 3.2 nC. The time needed to push or extract this charge with a given gate resistor is: $tson = \frac{Qg2 \cdot Rsource}{Vcc - Vplateau}$ (eq. 48) and $tsoff = \frac{Qg2 \cdot Rsink}{Vplateau}$ (eq. 49), with V_{CC} the lowest supply level delivered by the DSS (9.2 V). To minimize the EMI problems, the NCP1200 output impedance is asymmetrical: Rsource = 40 Ω (turn–on) while Rsink = 12 Ω (turn–off), as already accounted for in eq. 47 and 48. With these values, we obtain ts_{on} = 45 ns and ts_{off} = 6.4 ns. These numbers are rather low because of the small parasitic elements constituting the MTD1N60E. At the switch opening, the MOSFET current immediately drops thanks to a small ts_{off}. But the leakage inductance forces Ip to circulate through all the stray capacitance (Clump) and pulls up the drain with a slope of $\frac{Ip}{Clump}$ (eq. 50). Because the MOSFET is fully open when Vds rises, there are very few associated losses. In the case Vds (rising) and Ip (decreasing) would intersect together in their middle, the final P_{sw}off losses could be computed by: $P_{sw}off = \frac{Vds_{max} \cdot Ip_{max} \cdot ts_{off} \cdot Fsw_{max}}{6}$ (eq. 51) with Vds the highest drain–source level (600 V in worse case and without a clamping network). After computation, we obtain 14 mW a slightly optimistic number. The total power dissipation is thus: 440 mW + 175 mW + 14 mW = 630 mW, neglecting the gate losses. This number is below eq. 45 result and offers a comfortable *theoretical* security margin. We will confront these results with practical measurements on the board to ensure reliable operation.

Output Capacitor Selection

To evaluate the output capacitor value Cout, we need to define a given, acceptable level of ripple. The ripple finds its root in two different sources:

1. The natural integration of the secondary current (amputed by the DC current delivered to the load) through the capacitance gives birth to a capacitive voltage of $Vcap = \frac{1}{Cout} \cdot \int i_{(t)} \cdot dt$. This integral is valid during the secondary current decay until DCM is reached (Isec = 0). The remaining portion of time includes the dead–time (if any) plus the switch ON time.
2. The total parasitic contribution of Equivalent Series Resistor (ESR) and Inductor (ESL) that produce a voltage spike at every switch openings. The ESR contribution only is usually culprit for the majority of the ripple amplitude.

Thanks to simulation**,** Figure 9b is able to show these components separately and how they combine together:

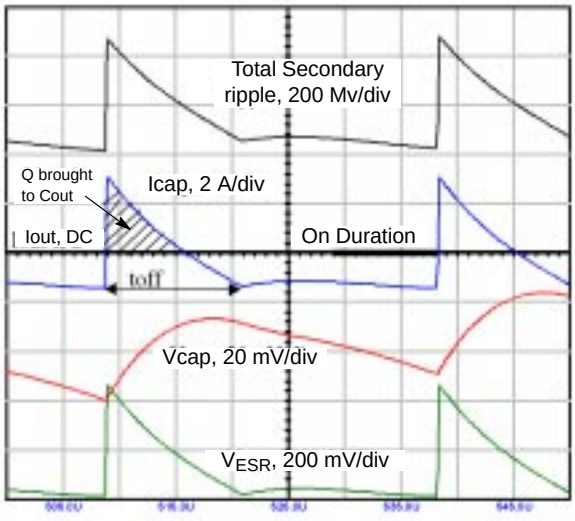

Figure 9b. The final ripple is made of the ESR and the output capacitance.

By looking at Figure 9b's INTUSOFT's IsSpice plot, we can evaluate the output capacitor voltage rise until the core is fully reset (t_{off} caption). First, let's calculate this t_{off} duration knowing that the secondary downslope is: $S_{sec} = \frac{(Vout + Vf) \cdot N^2}{Lp}$ or 405 mA/µs. With a secondary peak current Isec equal to N . Ip = 0.29 **.** 12.5 = 3.6 A, toff will last 8.9 µs for a 3.5 W nominal output power ($Iout_{DC}$ = 500 mA). With this value in mind, we can calculate the integrated voltage over Cout when subject to a ramping down current starting from (Isec – $Iout_{DC}$) and lasting 8.9 µs:

$$Vcap = \frac{1}{Cout} \cdot \int_0^{toff} \frac{toff - t}{toff} \cdot (Isec - Iout_{DC}) \cdot dt = \frac{toff}{2 \cdot C} \cdot (Isec - Iout_{DC})$$

. Thanks to this formula, we can extract the Cout value by: $Cout = \frac{toff \cdot (Isec - Iout_{DC})}{2 \cdot Vcap}$ or 490 µF with Vcap = 30 mV ripple. The simulation show higher ripple numbers because of an output power of 4.5 W.

Unfortunately, the ESR contribution is by far the higher contributor to the output ripple. This ohmic loss will generate a thin voltage spike equal to: R_{ESR} . (Isec–$Iout_{DC}$). In our case, a 100 mΩ ohmic loss produces up to 300 mV and adds up with the capacitor voltage ripple. The ESR also affects the capacitor dissipation by: $P_{Cout} = I^2_{capRMS} \cdot R_{ESR}$. You can smooth the ESR spike by inserting a secondary LC filter, as proposed by the various sketches of this application note.

Simulating the NCP1200

To ease your design phase, we have developed a transient and an AC averaged SPICE model for the NCP1200. Ready–to–use templates are available to download at www.onsemi.com in these three versions: INTUSOFT's IsSpice4, OrCAD's PSpice and Spectrum–Software's µCap. Describing these models is beyond the scope of this application note. However, we will show some typical waveforms you could quickly get with the help of these tools. Figure 10a portrays a typical IsSpice transient simulation using the NCP1200 in our 3.5 W charger application.

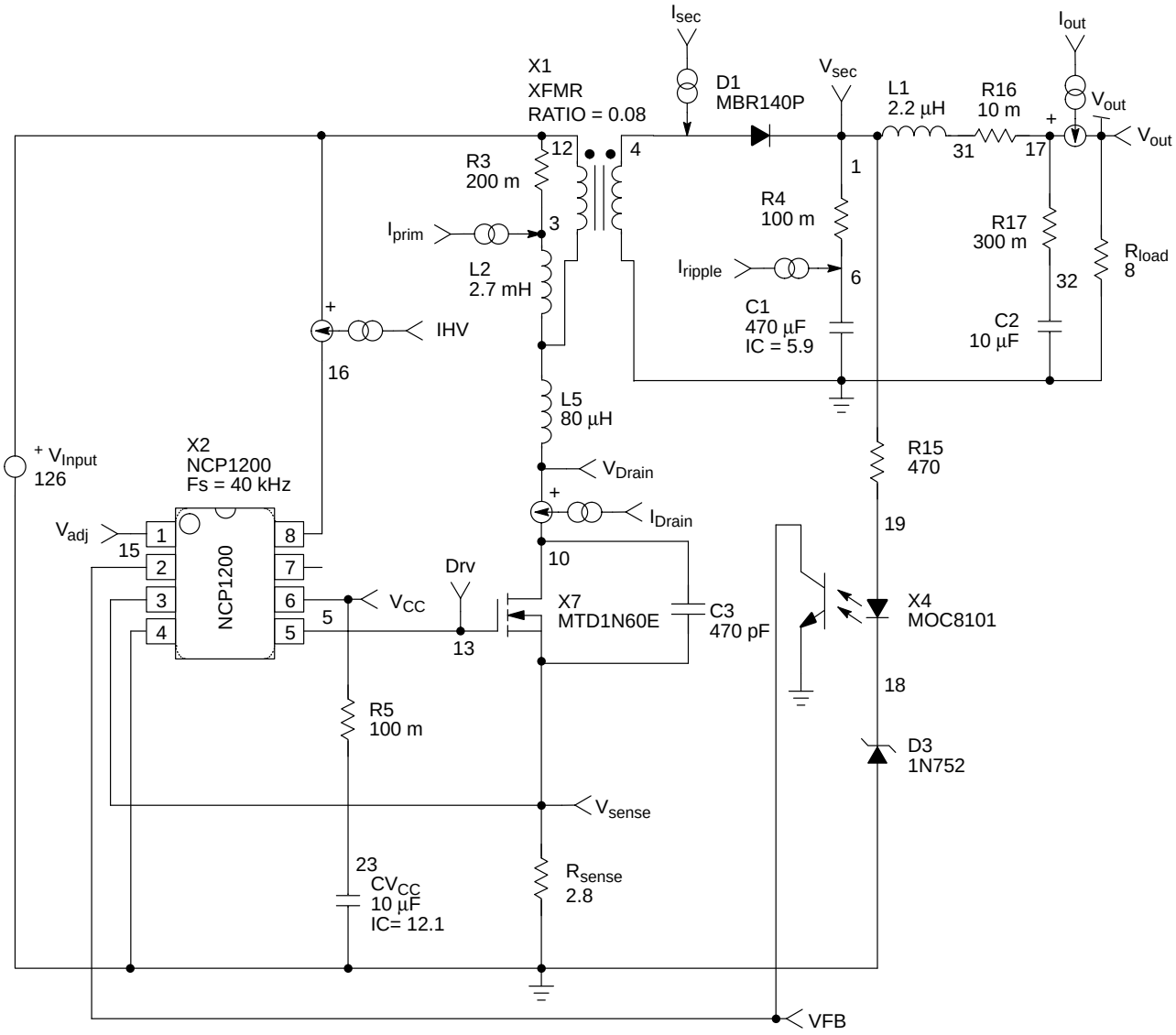

Figure 10a. A typical transient analysis of the NCP1200 with a dedicated SPICE model. C3 is purposely wired between drain–source to highlight the potential substrate injection problems.

The model includes the start–up source, various propagation delays, the short–circuit protection and the driver dual impedance concept. Typical waveforms are shown on Figure 10b and 10c. Thanks to short simulation times, the NCP1200 SPICE model will help you confirming the theoretical results you have already calculated.

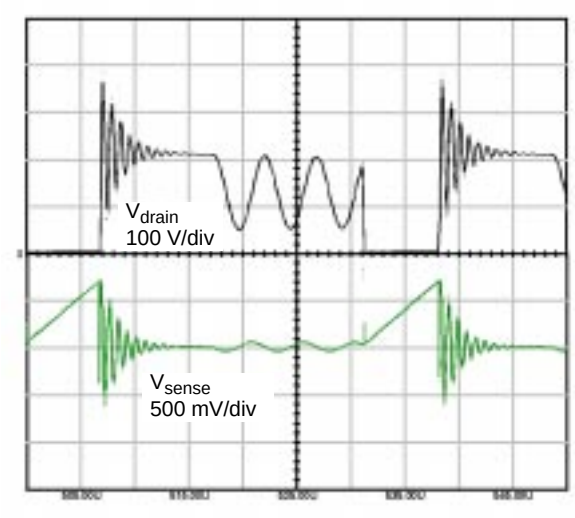

Figure 10b. Steady–State Drain–Source and Sense Voltages

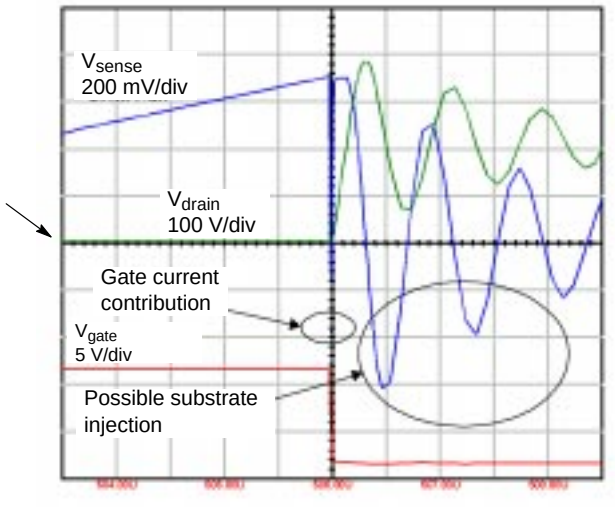

Figure 10c. Zoomed portion of MOSFET switch–off time when the snubber capacitor is wired between drain and source.

By feeding the various components with the choices you have made (e.g. transformer turn ratio), you can immediately verify that you do not exceed the safety limits. Such verifications could end–up into smoke on a real prototype test …

The Final Application Schematic

Figure 11a depicts the complete application schematic used in our NCP1200 AC/DC demoboard. Thanks to the weak leakage inductance exhibited by the transformer (≈80 μH), a simple capacitor in parallel with the MOSFET allows a safe operation up to 250 VAC, but to a slight detriment of switching losses (eq. 47).

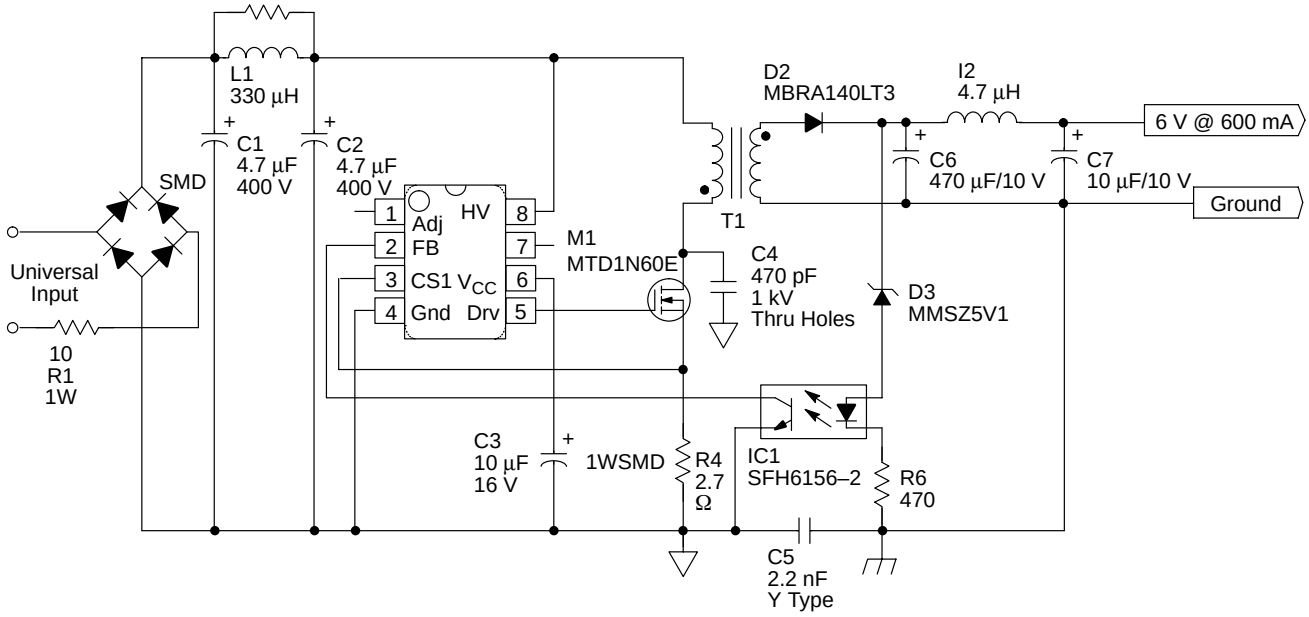

Figure 11a. The 3.5 W AC/DC adapter available as a demoboard

The PCB exhibits compact dimensions (64mm x 35mm) and includes a simplified EMI filter (L1). In case the common mode noise induced by M1 switching too fast exceeds the standard limits, you still have the option to slow it down a little bit by inserting a resistor between pin 5 and its gate. Below are some typical oscilloscope shots taken from the board:

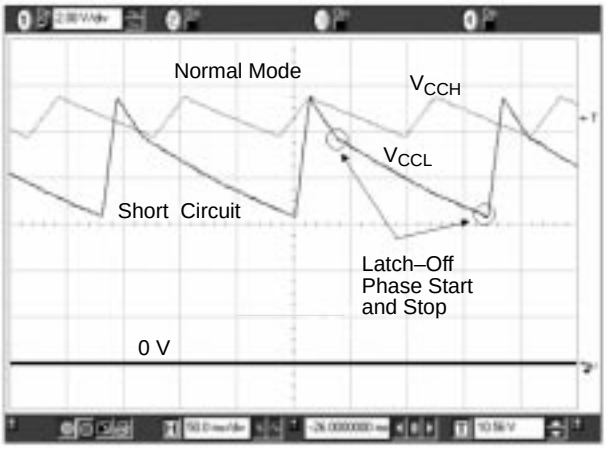

Figure 11b. The NCP1200 DSS behavior in normal and short circuit conditions.

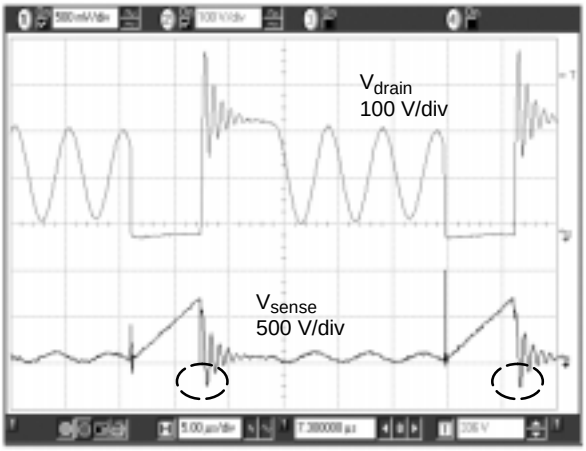

Figure 11c. Typical 3 W operation that can be compared to Figure 10b.

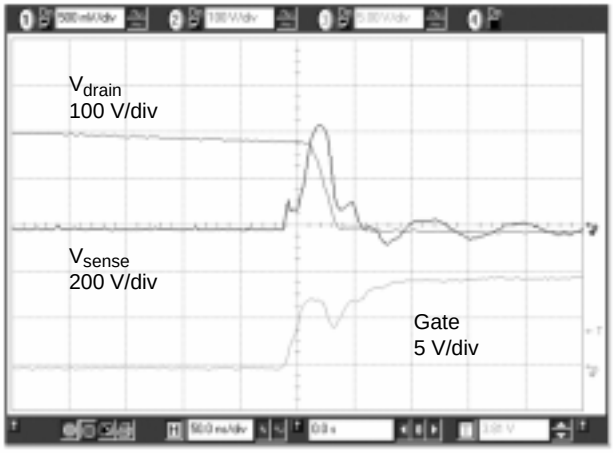

Figure 11c. This shot confirms our turn–on 45 ns calculation and shows the absence of immediate drain current. The capacitive peak is blanked with the NCP1200 LEB.

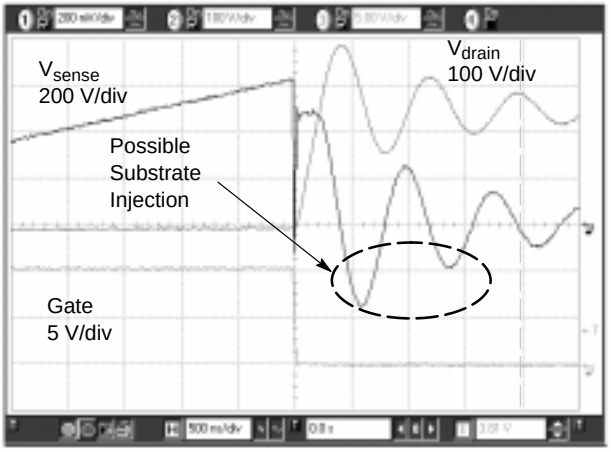

Figure 11d. As predicted by the calculations, the turn–off time is extremely fast and does not engender losses. The switch is immediately closed and the current is capacitive. This plot can be compared to Figure 10c.

Figure 11d represents the turn–off stage when the snubber capacitor is wired between drain and source. When the leakage starts to ring, the induced dV/dt forces a capacitive current to circulate inside the MOSFET Coss and the snubber. This current unfortunately creates a negative ringing over Rsense and can potentially inject into the NCP1200 substrate. This situation is highly undesirable as the injected electrons can go anywhere, possibly engendering an erratic behavior of the IC. To prevent this situation, simply wire the snubber between the drain and ground, as indicated by Figure 6b and confirmed by Figure 11e. In application where you do not install any snubber, the problem should not appear.

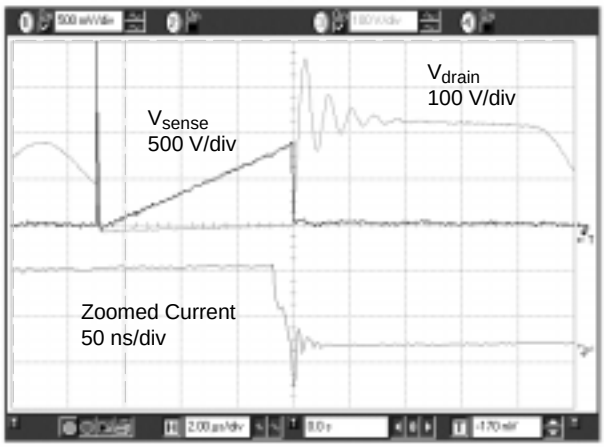

Figure 11e. Wiring the snubber between drain and source avoids the substrate injection.

However, in some higher power applications, the case can arise where the spike is present without the snubber in place. In that later case, we advise to wire a small low–pass RC filter between the sense resistor and pin 3. Typical values are R = 1 kΩ C = 220 pF. Another options lies in connecting a Schottky diode between pin 3 and ground (cathode to pin 3).

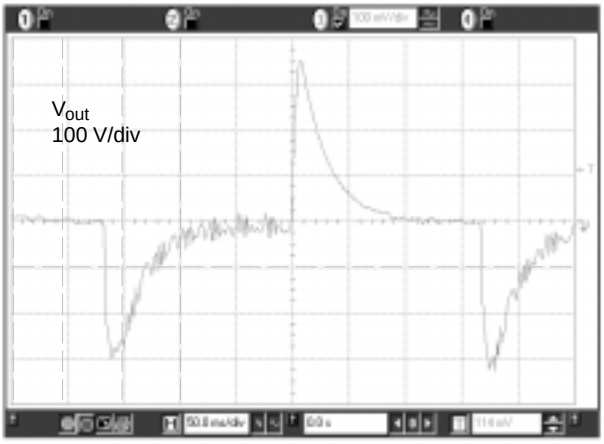

Figure 11f. Demoboard transient response when banged from 10 mA to 800 mA.

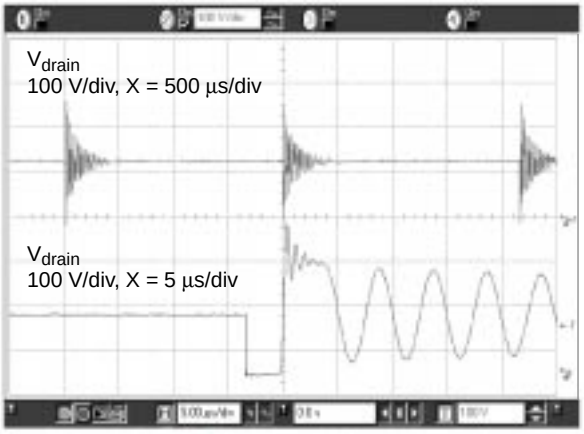

Figure 11g. Standby operation, upper curve is Vdrain with X = 500 μs/div.

Depending on the layout, the FB pin can pick–up some noise which leads to spurious oscillations. To cure this problem, wire a 1 nF capacitor between pins 2 and 4.

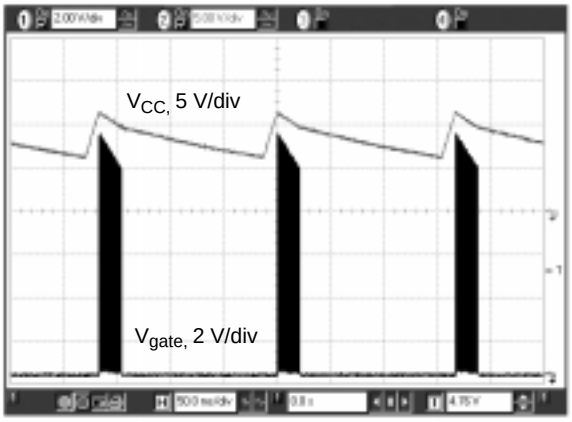

Figure 11h. Typical Operating Curves in Short–Circuit Conditions

Typical measurements on the 3.5 W AC/DC adapter:

DC Input Level	Input Power	Output Power	η
120	134 mW	0	–
120	732 mW	480 mW	65%
120	1.44 W	1.0 W	69.5%
120	4.08 W	3.3 W	80.6%
325	339 mW	0	–
325	1.06 W	480 mW	45%
325	1.84 W	1.0 W	54%
325	4.3 W	3.11 W	72%

At low line, the DSS contribution is low at about 100 mW. It represents nearly all the power consumption and does not significantly affect the efficiency. At higher line levels, because of the DSS constant current nature, its contribution increases and degrades the efficiency at weak output power levels. To greatly improve these numbers, you can apply Figure 2 trick or work with an auxiliary winding (Figure 3): it will save more than 200 mW. With the prototype under test, we measure an overload activation at a power level of 7 W.

Battery Charger Configuration

Certain applications require the control of the output current, e.g. battery chargers. To precisely monitor the output current flow, dedicated circuits already exist from ON Semiconductor such as the MC33341. This IC has been tailored to directly drive an SMPS optocoupler and turn your SMPS into a precise Constant Voltage–Constant Current (CV–CC) generator. For less precise requirements, Figure 12a depicts a configuration where a second loop has been added. This loop operates in parallel with the standard zener one and deviates the LED bias current to regulate the current (Q1 active). Of course, the current reference being the transistor Vbe, it is likely to change over temperature (–2.2 mV/°C)… However, this design can be selected where ± 10% current precision is enough. More precise designs can be made through a TL431 for better output precisions but also by combining the bipolar with a CTP to compensate the current loop temperature drift.

Figure 12a shows a typical configuration plugged into our NCP1200 averaged SPICE model. Thanks to this model, we can test for the open–loop stability by drawing a Bode plot of both loops (I or V) and transient test the validity of the CV–CC behavior:

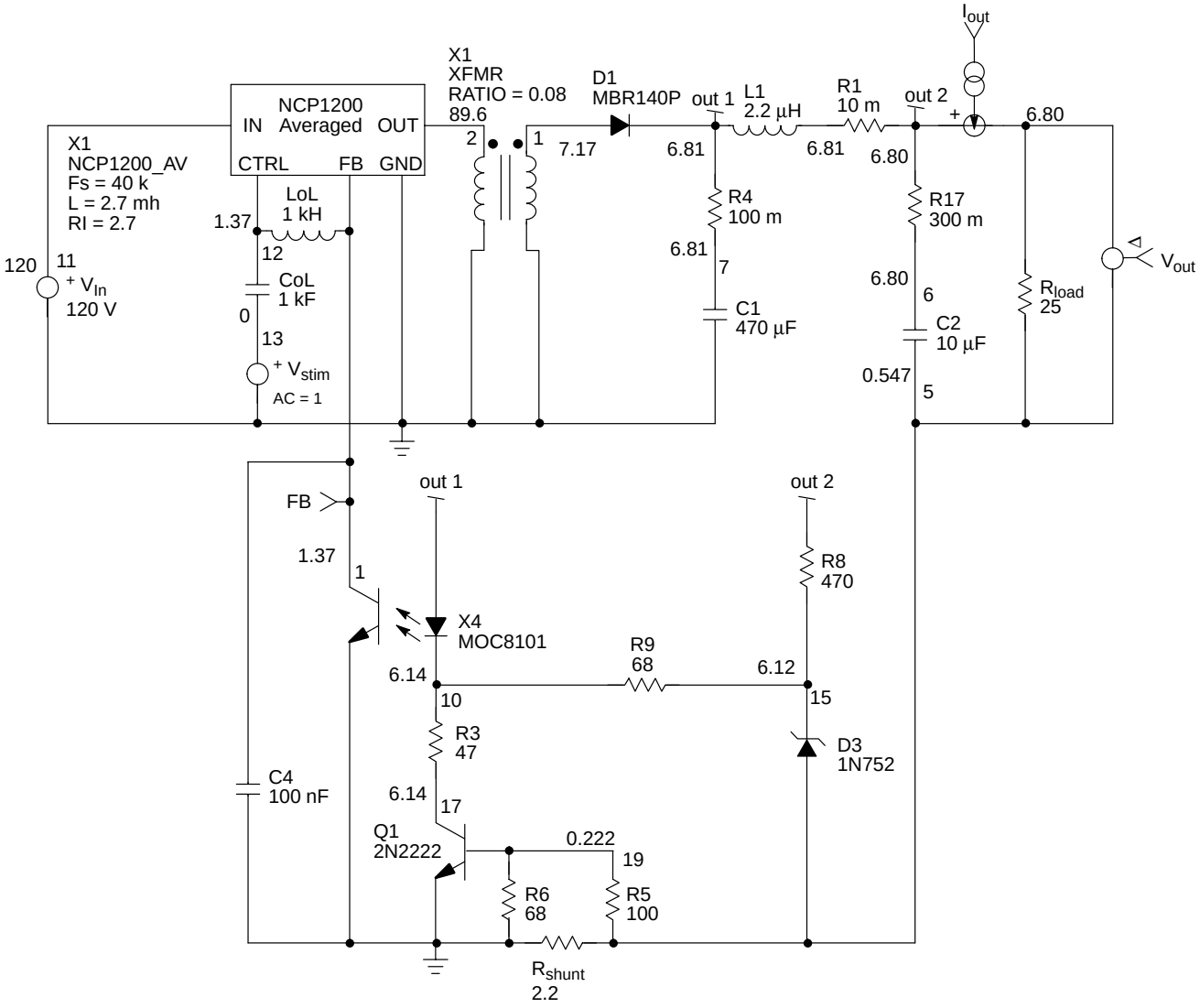

Figure 12a. An Averaged SPICE Simulation in a Battery Charger Application

By reflecting the bias points to the schematic, the simulator (IsSpice4 in this example), indicates which loop is active: the voltage loop in this case (Q1's Vbe is 203 mV and is off). By sweeping Vstim, Figure 12b and 12c reveal the Bode plot of the whole configuration where both loops have been represented.

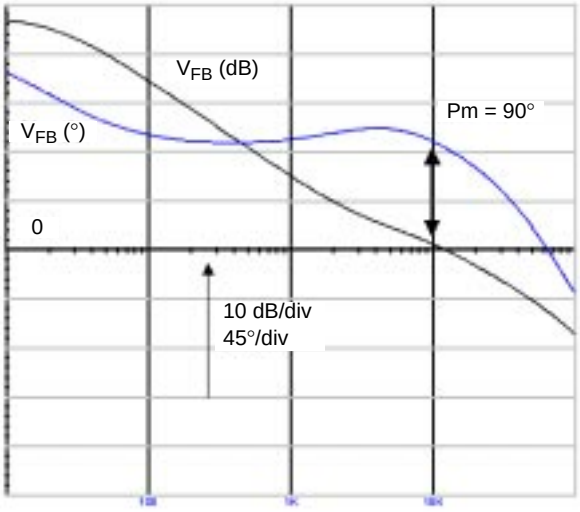

Figure 12b. The voltage sweep does not reveal any problem with a 90° PM...

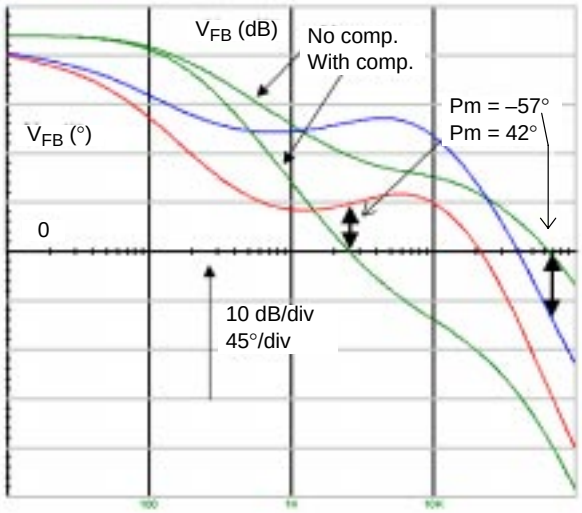

Figure 12c. However, the current loop is unstable with a large bandwidth.

As the below curves show, there is no problem when the voltage loop operates. The high gain finds one of its root in the NCP1200 internal collector resistance which equals 6.4 kΩ. But as you can see, it offers a good theoretical bandwidth associated with a safe phase margin. If we now activate the current loop, Figure 12c details a strong instability because of the bipolar presence. To cure this problem in the simplest manner, we can wire a 100 nF capacitor between FB and ground to roll–off the gain at lower frequencies. Updated Bode plots confirm the stability gained by this capacitor addition. This instability was observed on the evaluation board and also eradicated by the 100 nF capacitor.

By decreasing LoL and CoL elements down to 1p, we actually close the feedback loop. By sweeping the output load through a variable resistor, we plot the CC–CV curve as shown by Figure 12d.

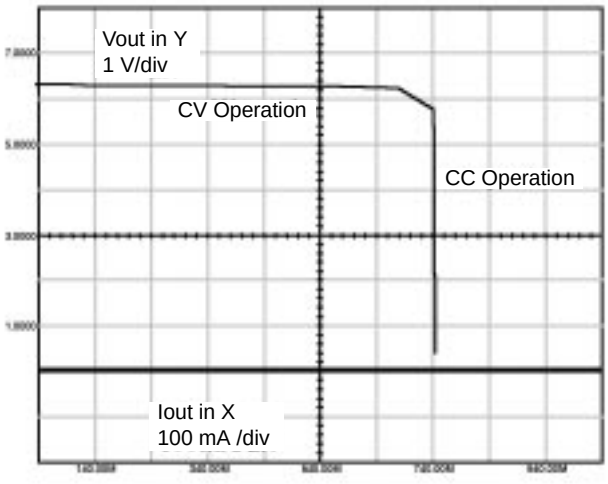

Figure 12d. The simulated CC–CV output shape as delivered by Figure 12a.

Please note that these average simulation circuits work with the demo versions of INTUSOFT, OrCAD and Spectrum–Software.

The complete battery charger schematic appears on Figure 13 and is available as another NCP1200 demoboard.

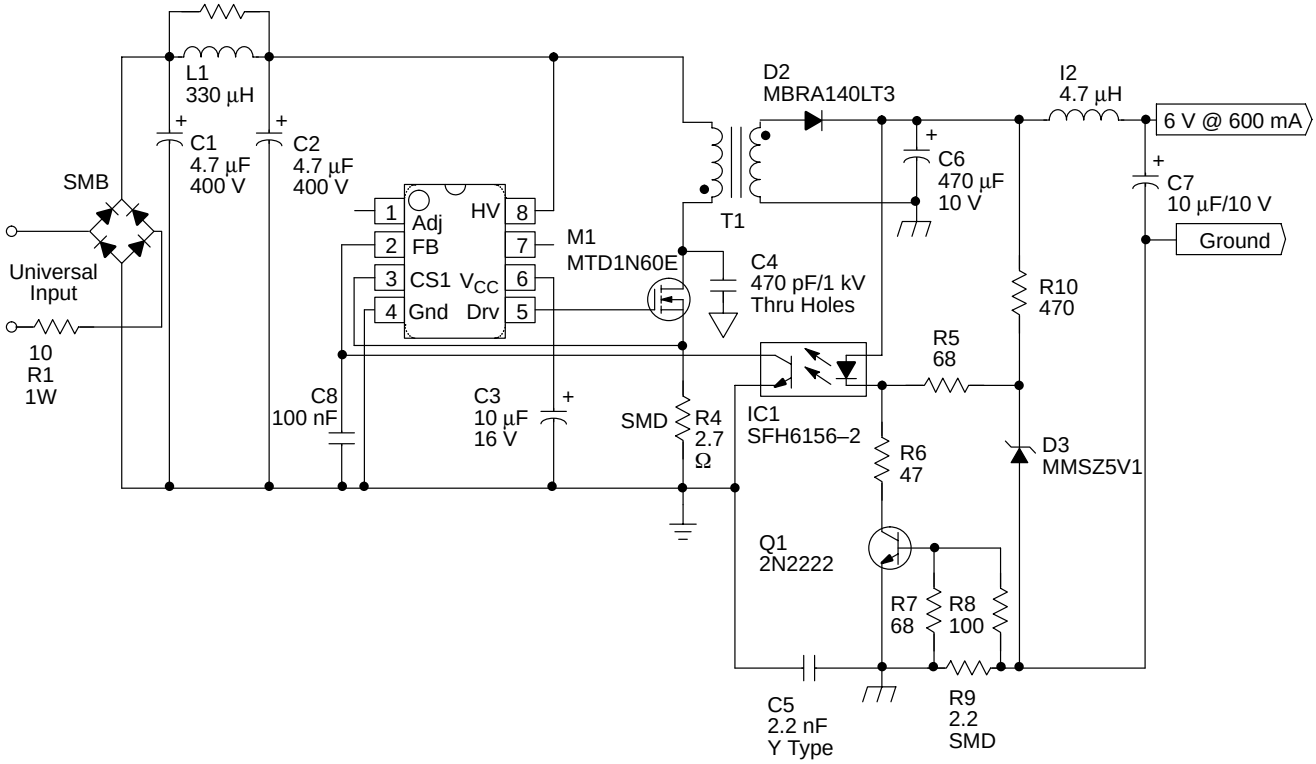

Figure 12e. The Complete Battery Charger Demonstration Board

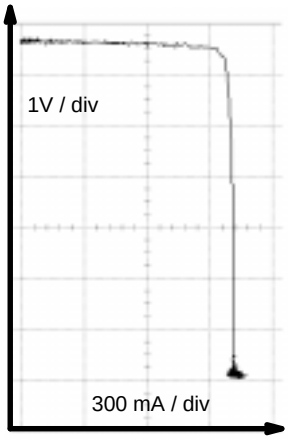

Figure 12f. The Resulting I–V Curve of the NCP1200 Charger Demoboard

Figure 12f depicts the resulting CV–CC obtained when sweeping the charger's output through a MOSFET and displaying the values with an X–Y oscilloscope.

Precise Secondary Regulation

Any TL431–based regulation scheme can be employed with NCP1200. Figure 13 gives in example the feedback section only when using a TL431 reference voltage. The TL431 is usually compensated by wiring a capacitor between the resistor bridge middle–point and the cathode. Different scheme will allow various bandwidth and response times. In that case, the averaged NCP1200 SPICE model appears as an invaluable tool to help you to place poles/zeroes at the correct location.

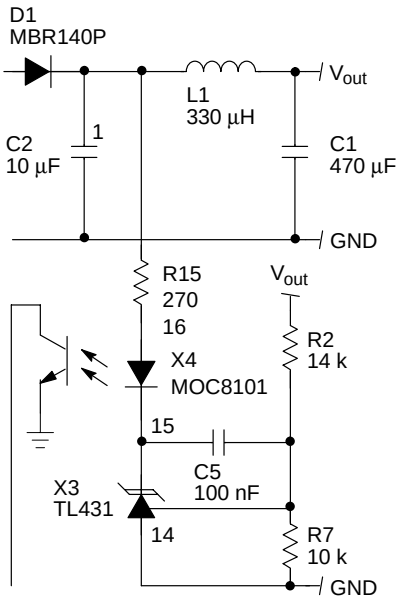

Figure 13. A Precise Regulation Option using a TL431 Reference Voltage

Primary Regulation Option

Despite the lack of internal error amplifier, two kind of primary regulation options can be implemented: one in which the short–circuit works as usual and another one where this option is permanently invalidated. Both options are depicted in Figure 13a and 13b sketches. To avoid classical peak rectification, a light load e.g. 470 Ω can be connected to load the auxiliary supply. Auxiliary and main power winding ratio should be adjusted to match the desired output voltage.

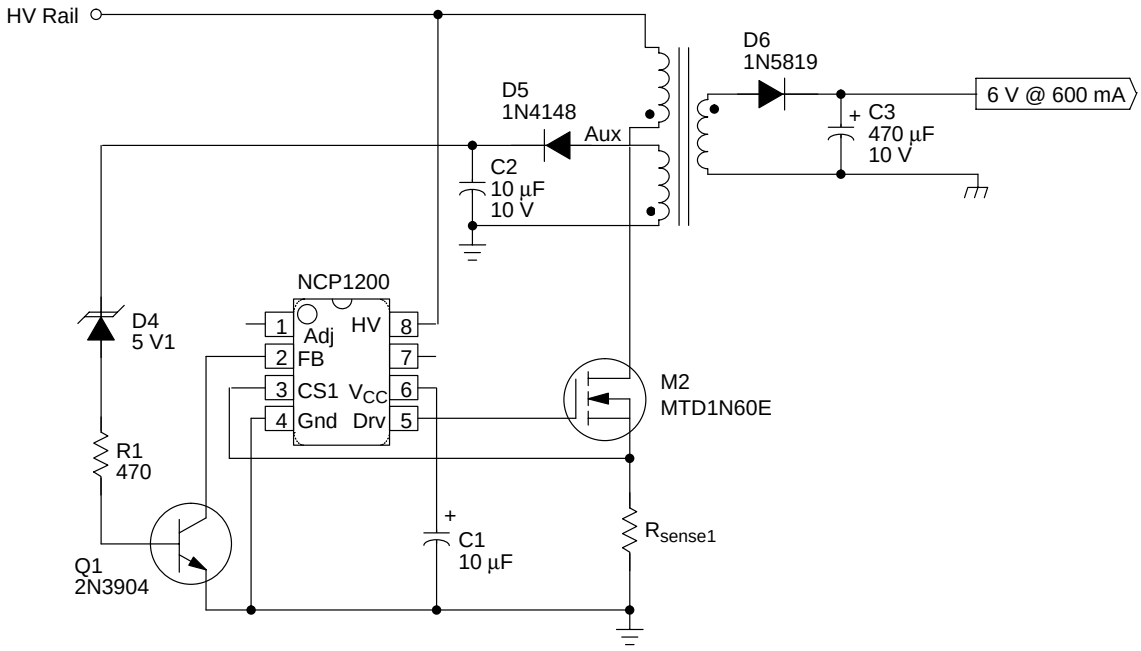

Figure 13a. A primary regulation possibility where the short–circuit protection still operates.

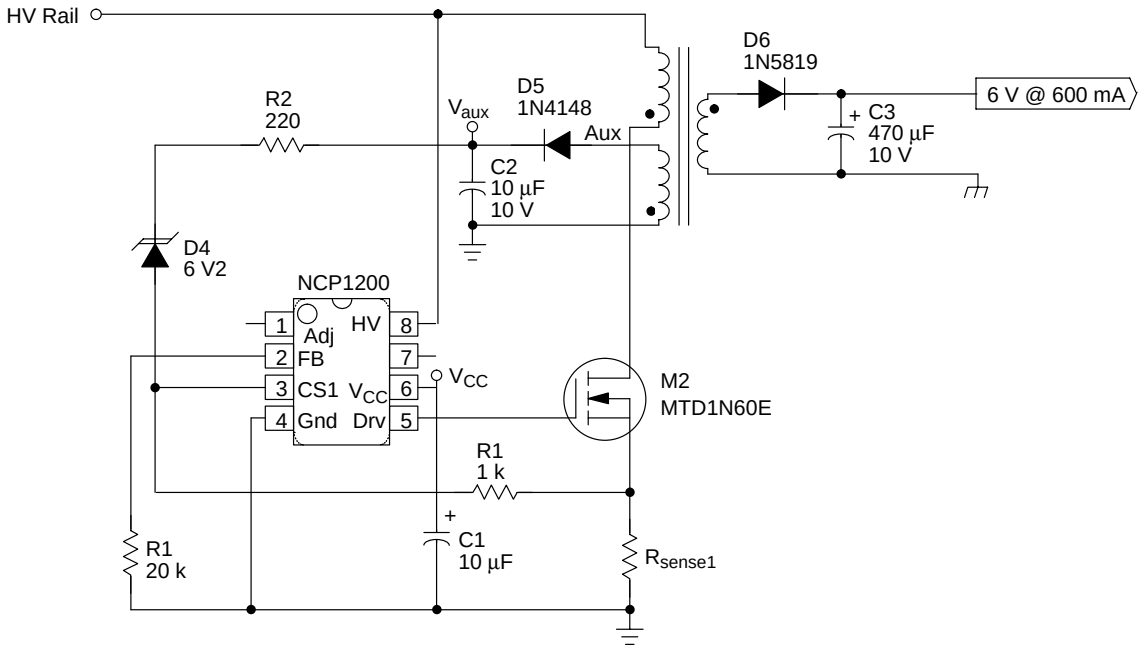

Figure 13b. Another primary regulation possibility where the short–circuit protection no longer operates.

Transformer Availability

T1 transformer for the depicted circuits (charger and AC adaptor) is immediately available from several manufacturers whose details are given below. The 2.7 mH E16 version corresponds to a 3.5 W charger operating with an NCP1200P40 (40 kHz) while the 1.8 mH version should be used for a 5 W NCP1200P60 version (60 kHz).

Eldor Corporation Headquarter
Via Plinio 10,
22030 Orsenigo
(Como) Italia
Tel.: +39–031–636 111
Fax : +39–031–636 280
Email: eldor@eldor.it
www.eldor.it

ref. 1: 2262.0058C: 3.5 W version
(Lp = 2.9 mH, Lleak = 80 μH, E16)
ref. 2: 2262.0059A: 5 W version
(Lp = 1.6 mH, Lleak = 45 μH, E16)

EGSTON GesmbH
Grafenbergerstraβe 37
3730 Eggenburg
Austria
Tel.: +43 (2984) 2226–0
Fax : +43 (2984) 2226–61
Email: info@egston.com
http://www.egston.com/english/index.htm

ref. 1: F0095001: 3.5 W version
(Lp = 2.7 mH, Lleak = 30 μH, sandwich configuration, E16)

Atelier Special de Bobinage
125 cours Jean Jaures
38130 ECHIROLLES FRANCE
Tel.: 33 (0)4 76 23 02 24
Fax: 33 (0)4 76 22 64 89
Email: asb@wanadoo.fr

ref. 1: NCP1200–10 W–UM: 10 W for USB
(Lp = 1.8 mH, 60 kHz, 1:0.1, RM8 pot core)

Coilcraft
1102 Silver Lake Road
Cary, Illinois 60013 USA
Tel: (847) 639–6400
Fax: (847) 639–1469
Email: info@coilcraft.com
http://www.coilcraft.com

ref. 1: Y8844–A: 3.5 W version
(Lp = 2.9 mH, Lleak = 65 μH, E16)
ref. 2: Y8848–A: 10 W version
(Lp = 1.8 mH, Lleak = 45 μH, 1:01, E core)

SPICE Editors

As mentioned in the text, NCP1200 ready–to–use SPICE platforms are available to download from the ON Semiconductor Web site in the following formats: OrCAD's PSpice, INTUSOFT's IsSpice and Spectrum–Software's μCap. You will find both transient and AC analysis templates as described by Figures 10a and 12a. Some of these examples can work on the editor's demo versions, some will require the full version to operate. Editors demo versions can be downloaded at the following locations: www.orcad.com (PSpice), www.intusoft.com (IsSpice) and www.spectrum–soft.com (μCap).

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303–675–2167 or 800–344–3810 Toll Free USA/Canada

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German Phone: (+1) 303–308–7140 (Mon–Fri 2:30pm to 7:00pm CET)
Email: ONlit–german@hibbertco.com
French Phone: (+1) 303–308–7141 (Mon–Fri 2:00pm to 7:00pm CET)
Email: ONlit–french@hibbertco.com
English Phone: (+1) 303–308–7142 (Mon–Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL–FREE ACCESS*: 00–800–4422–3781
*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:
Spanish Phone: 303–308–7143 (Mon–Fri 8:00am to 5:00pm MST)
Email: ONlit–spanish@hibbertco.com
Toll–Free from Mexico: Dial 01–800–288–2872 for Access – then Dial 866–297–9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 1–303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.